VHDL, or, HOW I LEARNED TO STOP OVERTHINKING THINGS AND BUILD AN ALU

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PROJECT
self-directed 300-level course in machine organization

learned: VHDL, Xilinx, ModelSim
created: counters, flip-flops, ALU, CPU, testbenches
programmed: Spartan-3 FPGA with 4-bit ALU

Sample Code

entity cpu is
Port(dataout: out word;
datain: in word;
dataout: out word;
readStrobe, writeStrobe: out bit;
reset: in bit;
clk: in bit);
end cpu;
architecture interpreter of cpu is
signal stub : bit;
signal sdatain : word;

VHDL
a hardware description language used to describe digital systems & implement them using devices such as field programmable gate arrays (FPGAs)

XILINX SDK
an integrated design environment for embedded systems

MODELSIM
used to simulate & analyze the behavior of VHDL constructs on sample inputs & outputs

WHY?
flexible & customizable: allow for reconfigurable systems to fit the task at hand
cost: no need for a new chip for each project

Why?

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